

CLAIMS

What is claimed is:

- 1 1. A layout comprising for an even number of discrete transistors, N,
2 comprising:
 - 3 a first half of the transistors ($N/2$) oriented along a first axis,
 - 4 a second half of the transistors ($N/2$) oriented along a second axis
5 orthogonal to the first half of the transistors.
- 1 2. The layout of claim 1, wherein the transistor layout is bilaterally
2 symmetric along both the X and Y axis.
- 1 3. The layout of claim 1, comprising:
 - 2 a plurality of legs arranged in a bilaterally symmetric format, the legs
3 forming the gates of the N transistors.
- 1 4. The layout of claim 3, further comprising:
 - 2 diffused areas forming sources and drains; and
 - 3 an area at which any of the plurality of legs cross, the area being a non-
4 diffused area.
- 1 5. The layout of claim 3, wherein the plurality of legs form a tic-tac-
2 toe pattern.
- 1 6. The layout of claim 5, wherein
2 the tic-tac-toe pattern defines square areas between the legs; and

3 the source and drain areas alternate in the square areas.

1 7. The layout of claim 5, wherein the tic-tac-toe pattern may be
2 repeated to form a larger layout.

1 8. The layout of claim 1, used for an integrated circuit, wherein the
2 gate orientation reduces skew effects due to mask alignment and gate
3 orientation.

1 9. A symmetric transistor layout comprising:
2 an even number of transistor legs, laid out in an intersecting pattern,
3 forming a bilaterally symmetric base;
4 a plurality of source areas and drain areas defined by rectangles enclosed
5 by two or more transistor legs; and
6 undiffused areas defined by an intersection of the legs;
7 a plurality of transistors defined by a portion of a leg forming a gate and
8 the source and drain areas on either side of the leg forming a source and a drain.

1 10. The symmetric transistor layout of claim 9, wherein the plurality of
2 transistors is an even number of transistors.

1 11. The symmetric transistor layout of claim 10, wherein a first half of
2 the transistors are horizontally oriented and a second half of the transistors are
3 vertically oriented.

1 12. The symmetric transistor layout of claim 9, wherein the plurality of
2 legs form a tic-tac-toe pattern.

1 13. A method of making a symmetric transistor device comprising:
2 depositing a first conductive layer on a substrate, the first conductive
3 layer forming an even number of transistor legs, laid out in an intersecting
4 pattern, forming a bilaterally symmetric base;
5 doping the substrate to form source and drain regions; and
6 forming a plurality of transistors defined by a portion of a leg forming a gate and the source and drain areas on either side of the leg forming a source and
7 a drain.

1 14. The method of claim 13, further comprising:
2 depositing a silicon dioxide prior to depositing the first conductive layer.

1 15. The method of claim 13, wherein a diffusion plate used for doping
2 forms undoped areas at intersections of the transistor legs.

1 16. The method of claim 13, wherein the intersecting pattern forms a
2 tic-tac-toe pattern.

1 17. The method of claim 13, wherein the first conductive layer
2 comprises polysilicon.

1 18. The method of claim 13, further comprising:

2 conductive interconnections between the source and drain areas to form a
3 circuit.

1 19. The method of claim 13, wherein a first half of the transistors are
2 oriented along a first axis and a second half of the transistors (N/2) oriented
3 along a second axis orthogonal to the first half of the transistors.

1 20. The method of claim 19, wherein the minimum drawn W/L is used
2 for each transistor leg.